REMARKS

Claims 1–20 are pending in the present application.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 103 (Obviousness)

Claims 1–20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,127,091 to *Boufarah et al* in view of U.S. Patent No. 6,289,445 to *Ekner*. This rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142, p. 2100-128 (8th ed. rev. 2 May 2004). Absent such a *prima facie* case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.*

To establish a *prima facie* case of obviousness, three basic criteria must be met: First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *Id.*

Independent claims 1, 8 and 15 each recite a fetch-branch unit and a decode unit. In addition,

claim 8 further recites at least one execution unit. Such a combination of features is not found in the cited references. *Boufarah et al* depicts an instruction fetching and branch processing unit 14, a fixed point processing unit 20, and other processing units 22. However, *Boufarah et al* does not depict a separate decode unit, but instead teaches that instructions are decoded in the fixed point execution unit 22. *Boufarah et al*, column 4, lines 9–10. Thus *Boufarah et al* does not disclose "a decode unit," separate and distinct from execution unit(s).

Independent claims 1, 8 and 15 also each recite that the fetch-branch unit and decode units operate in parallel, both receiving the same instruction(s) during a given cycle and having the sequential and target instructions retrieved thereto concurrently. Such a feature is not found in the cited references. As conceded in the Office Action, such a feature is not found in *Boufarah et al*. Contrary to the assertion within the Office Action, such a feature is also not found in *Ekner*. The cited portion of *Ekner* depicts a unit 304 decoding instructions and detecting branch instructions operating in series with a fetch unit 302:

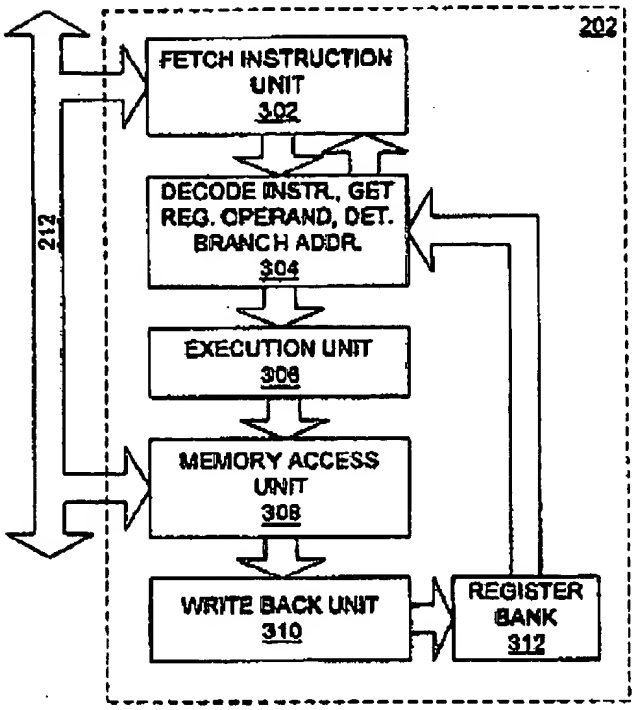

FIG. 2

Ekner, Figure 2, column 5, lines 52–65. *Ekner* thus teaches a fetch unit and a decode-branch unit, not a fetch-branch unit and a decode unit as recited in the claims. Furthermore, instructions are NOT received concurrently at the fetch unit 302 and the decode-branch unit 304 in *Ekner*, as recited in the claims.

In addition, *Ekner* teaches speculative execution of instructions, but does not teach fetching instructions from both sequential and target locations for a branch instruction during the two clock

cycles following detection of the branch instruction. Accordingly, the references do not provide a reasonable expectation of success in combining the teachings selected therefrom as proposed in the Office Action.

Claims 2, 9 and 16 each recite dropping either the sequential instruction or the target instruction from both the fetch-branch unit and the decode unit upon resolving the branch instruction. Such a feature is not found in the cited references. *Boufarah et al* teaches speculatively decoding and executing the sequential instructions, which are purged if the branch is taken and the target instructions are to be executed instead. *Boufarah et al*, column 4, line 29 through column 5, line 60. To the extent the processing unit 20 is taken as satisfying the recited limitation of "a decode unit," *Boufarah et al* does not teach dropping either the sequential instructions or the target instructions from both the fetch-branch unit and the decode unit upon resolution of the branch instruction as recited in the claims. In the system disclosed by *Boufarah et al*, if the sequential instructions are to be executed, the target instructions are never forwarded to the processing unit 20 for execution, and therefore cannot be "dropped" from the processing unit 20 as well as the fetch-branch unit 14; on the other hand if the target instructions are to be executed, the sequential instructions are purged only from the processing unit 20 in response to resolution of the branch instruction, not from both fetch-branch unit 14 and processing unit 20 (those sequential instructions having previously been eliminated from fetch-branch unit 14 during transfer to the processing unit 20).

Claims 4–7, 11–14 and 18–20 each recite marking instructions with various identifiers:

regular, branch, sequential and/or target. Such a feature is not found in the cited references. The labels "X1," "X2," "BRC" and "S1" through "S3" within *Boufarah et al* are simply references used to identify the respective types of instructions for the purposes of description. Nowhere does *Boufarah et al* teach marking the instructions with those identifiers. Identifying instructions as one of the types of instructions described does not constitute "inherent" marking of the instructions as asserted in the Office Action. Moreover, the claim requires explicit marking of the instruction types, to facilitate purging of either sequential or target instructions.

Therefore, the rejection of claims 1–20 under 35 U.S.C. § 103 has been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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